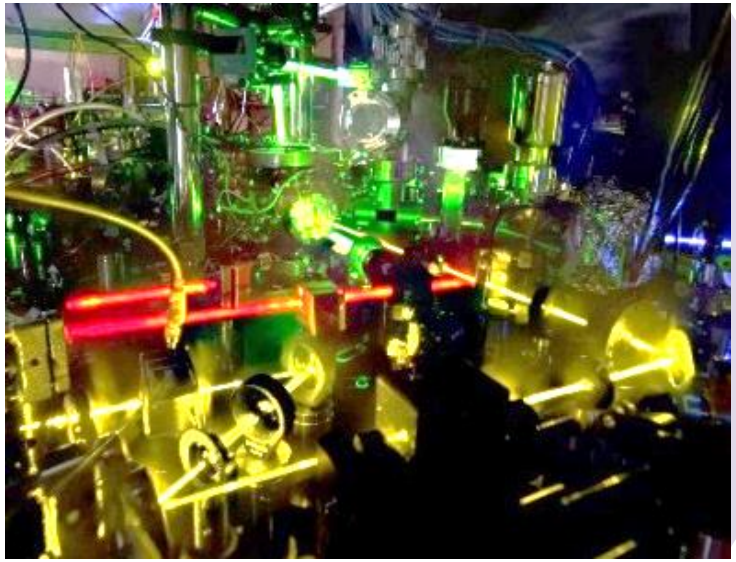
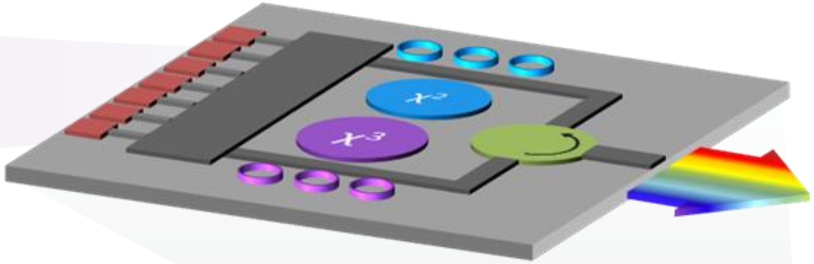
Lasers for Universal Microscale Optical Systems (LUMOS)

Gordon Keeler, PM, DARPA/MTO

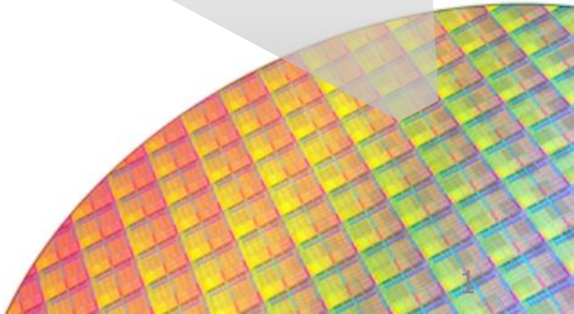


courtesy NIST



Proposer's Day

November 20, 2019

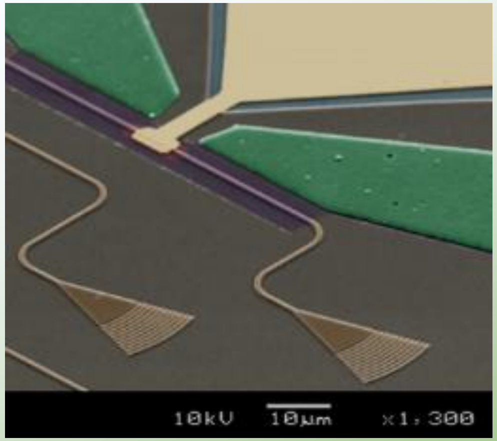


https://beta.sam.gov/opp/e9c6db5a6fc44a789ebdea6b77166207/view

Integrated Photonics and Optical Microsystems

Wide application space for impact

- Numerous mission areas of interest within the DoD
- Technology investment & development will enable new capabilities

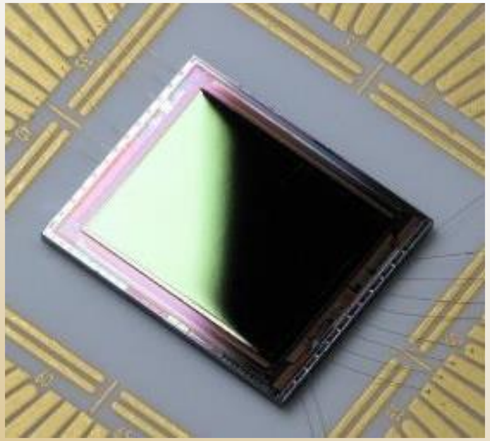


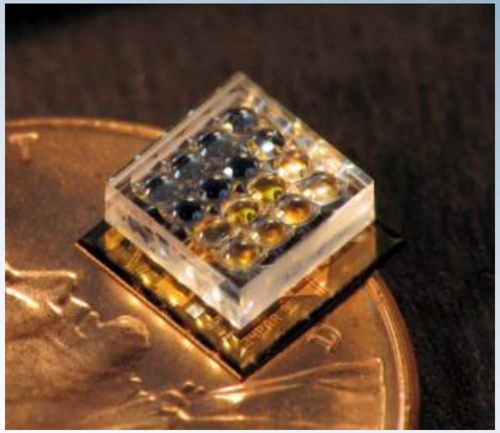
Information

Comms: fiber, free-space
RF: processing, remoting
Quantum: computing, comms

Vision

Imaging: EO/IR, spectral
Active imaging: LIDAR
Display: HUD, holographic



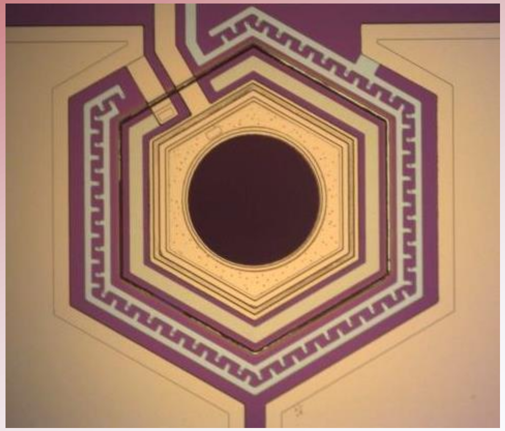


Microsensors

Detection: chem, bio, rad
Position: gyros, accel, TTL
Timing: atomic clocks

Energy

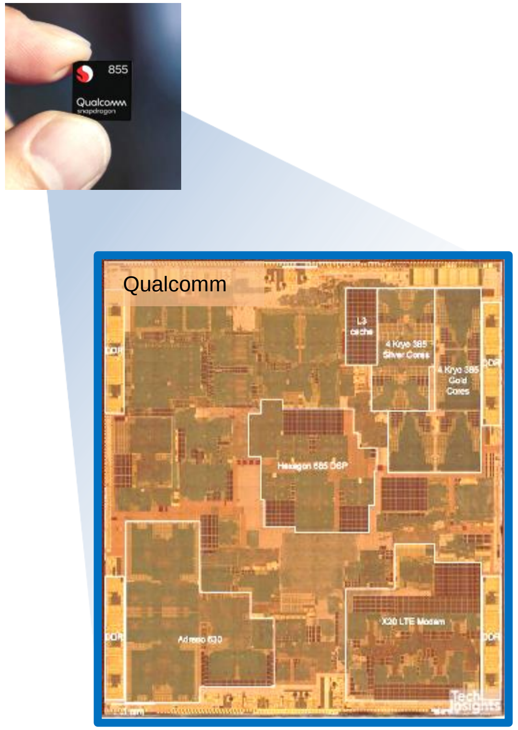
Power: delivery, harvesting
Signatures: emissivity control
High energy: directed & CM



all images courtesy Sandia National Laboratories

Integrated Gain Enables Scalability

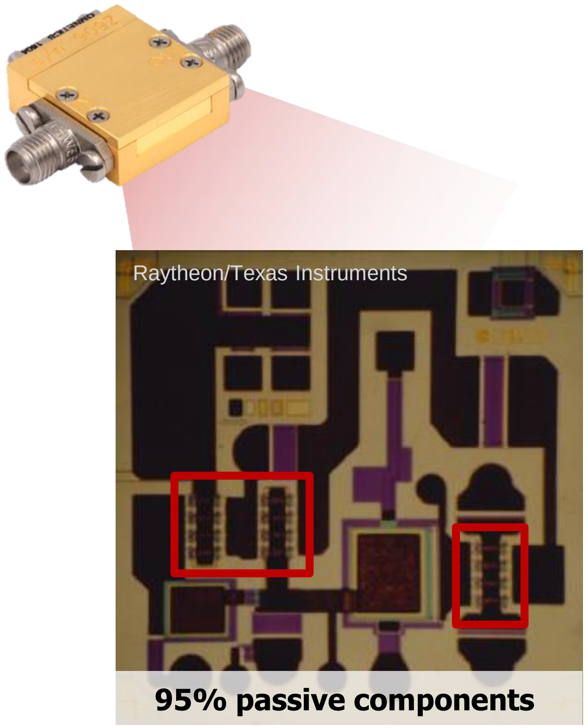
Digital Electronics



CMOS
integrated circuit

ON-chip gain
enables logic complexity scaling
through transistor fan-out

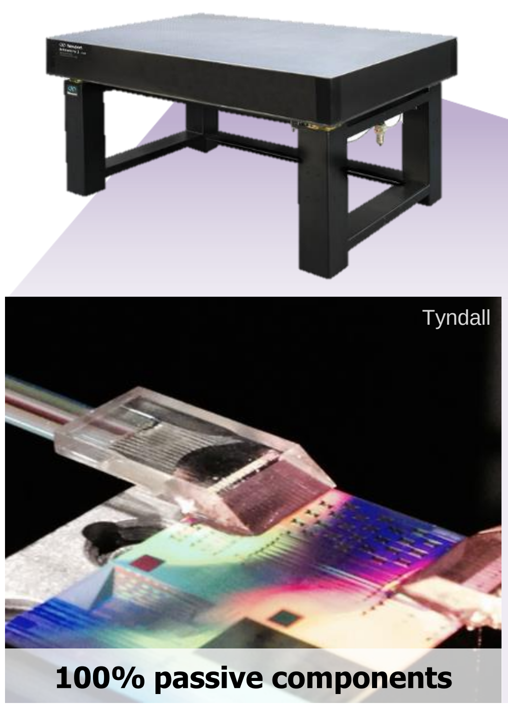
Microwave Electronics



microwave
integrated circuit

ON-chip gain
enables RF power scaling
for radar & communications

Typical Photonic Solutions



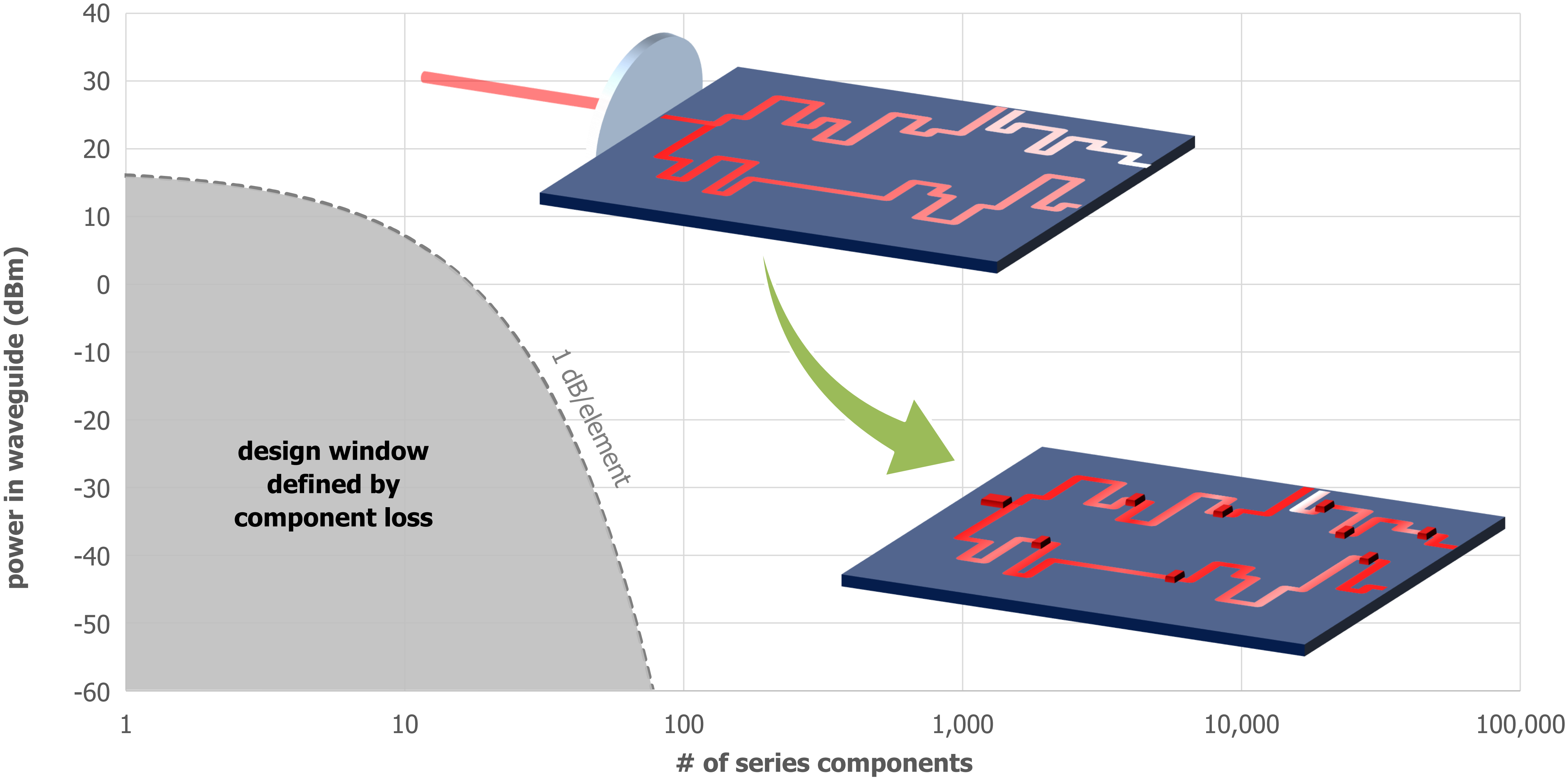
+

photonic
integrated circuit

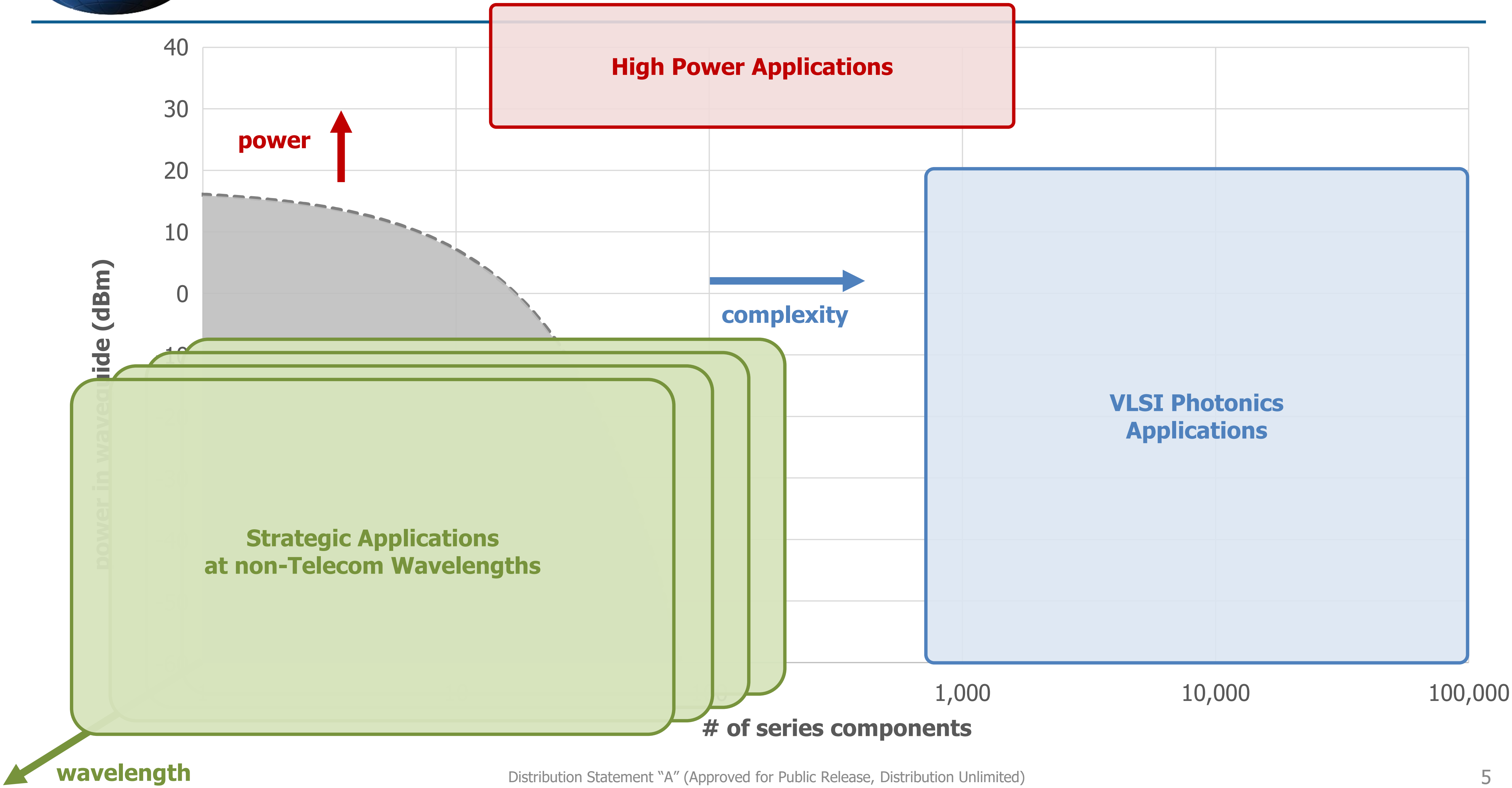
external photon sources &
high-end components
(lasers, amplifiers, modulators, isolators, detectors…)

OFF-chip gain
severely limits performance
and dominates system C-SWaP

Optical Losses Limit Impact

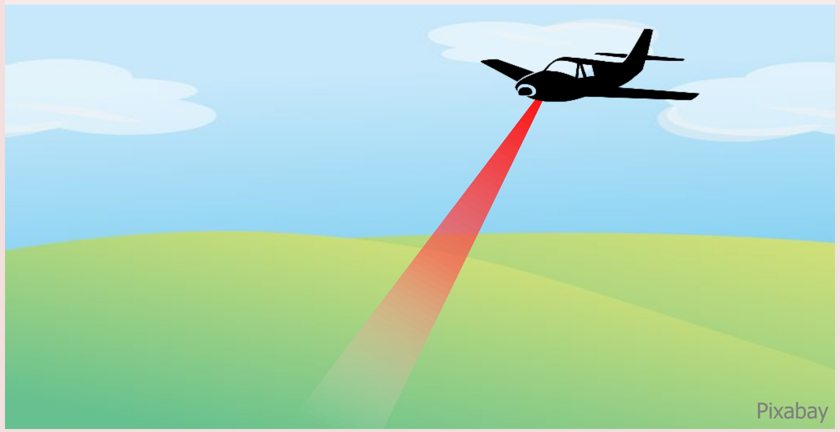


Scaling for New Applications

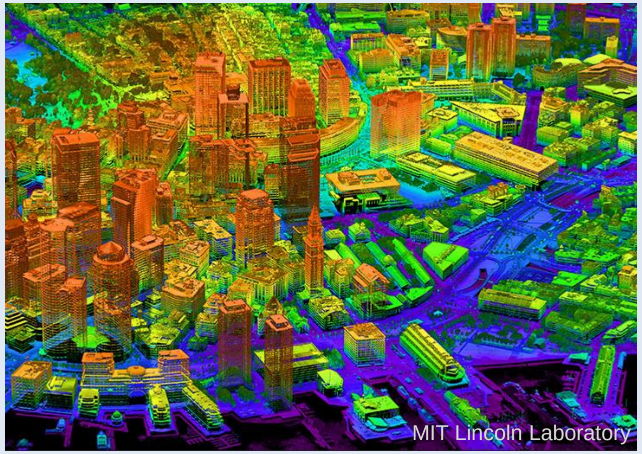


LUMOS: Domains of Impact (see BAA for others)

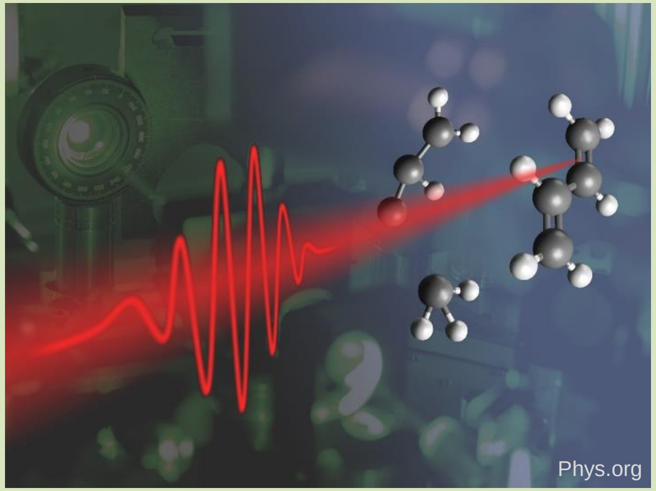
Power: RF Processing and Remote Sensing



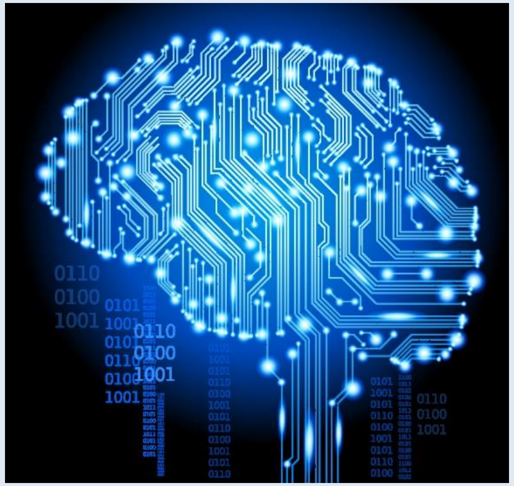
Foundry Integration: Compact Sensing



Spectrum: Atomic, Chem/Bio & Quantum Sensing



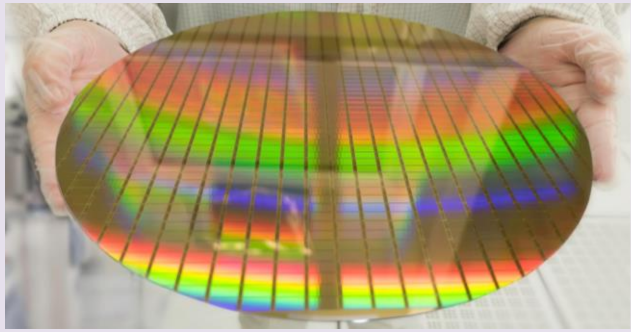
Complexity: Information Processing



Technical Areas

LUMOS Overview

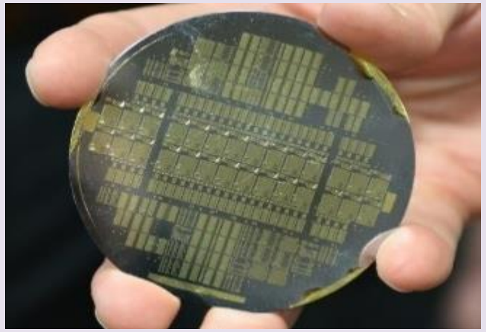
Best Integrated Circuits (Si, $LiNbO_3$, SiN, …)



X Gain
- no native gain due to material limitations

✓ Photonics
- excellent yield and manufacturability

Best Lasers (GaAs, InP, GaN, …)



https://innovationorigins.com/what-to-expect-from-european-photonics-in-2019/

✓ Gain
- discrete lasers & amplifiers
- high power, efficiency & lifetime

X Photonics
- low density & low yield
- high optical losses

LUMOS

intimate integration of gain materials and high-performance photonics

TA1: Scaling Complexity with Gain

Gain: Many efficient, high-density gain blocks
Photonics: Advanced process with foundry access

TA2: High Power Gain

Gain: Watt-class lasers and amplifiers
Photonics: Fast analog components with low loss

TA3: Broad Spectrum Gain

Gain: Narrow linewidth across a wide spectrum
Photonics: Full functionality over visible wavelengths

Bring efficient on-chip optical gain to highly-capable integrated photonics platforms for disruptive optical microsystems

Program Structure

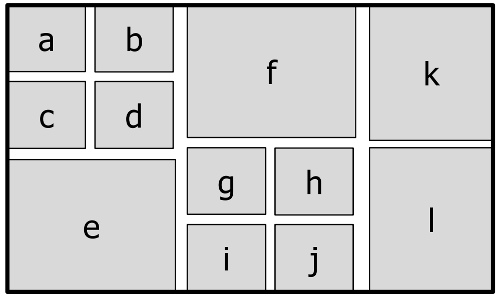
FY20	FY21	FY22	FY23	FY24

Phase 1 (18 months) → **Phase 2 (18 months)** → **Phase 3 (12 months)**

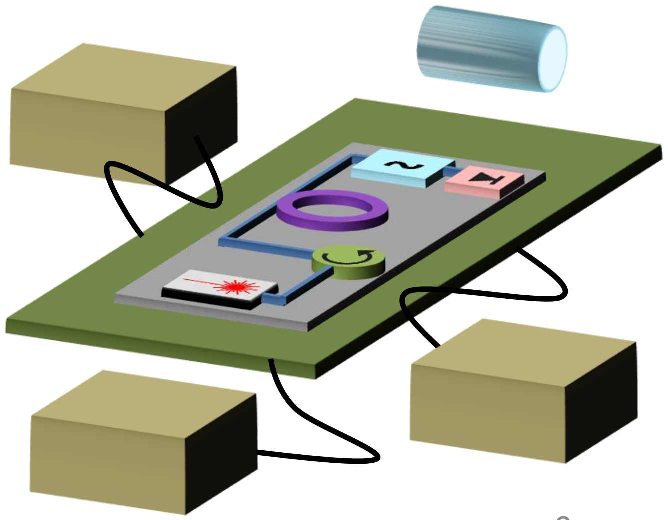
Gain integration development

Optimization and platform integration

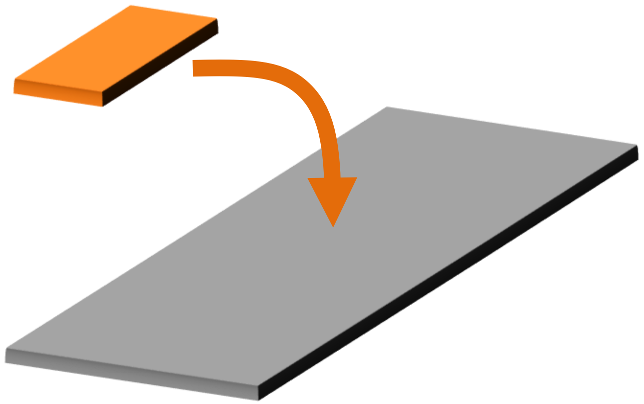
TA1: User Access

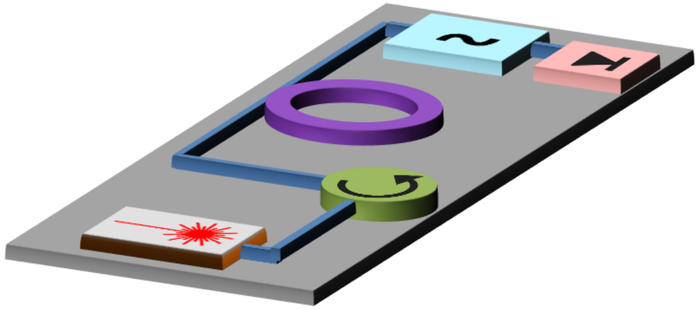


TA2/3: System Demo



TA1: Scaling Complexity with Gain





TA2: High Power Gain

TA3: Broad Spectrum Gain

TA1: Scaling Complexity with Gain

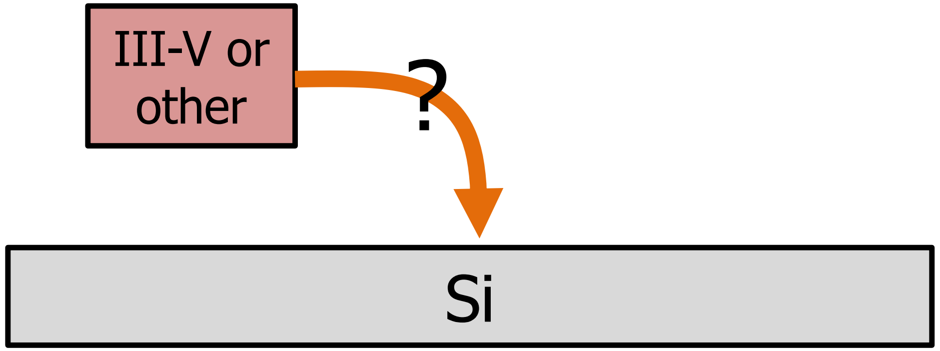
Objectives

- Enable **disruptive scaling for VLSI photonics** by integrating dense and flexible gain
- Expand the **performance and capability of Si photonics**
- Establish **access to integrated gain** through PDK and MPWs

Key Metrics and Deliverables

- Demonstrate **on-chip lasers** and **optical amplifiers**
  - **1,000** gain blocks per reticle (100x SOTA)
  - 16 dBm lasers at 40% efficiency
  - Flexible and variable gain blocks
- Enable **low loss waveguides** in foundry
  - 0.05 dB/cm SiN loss
- Facilitate access through **PDKs** and **MPW runs**
  - DoD user community exercises process through MPW runs
  - 8" or 12" foundry platform

Accessible Integrated Optical Gain Capability



TA1 will enable dramatic PIC scalability through gain integration in a silicon foundry

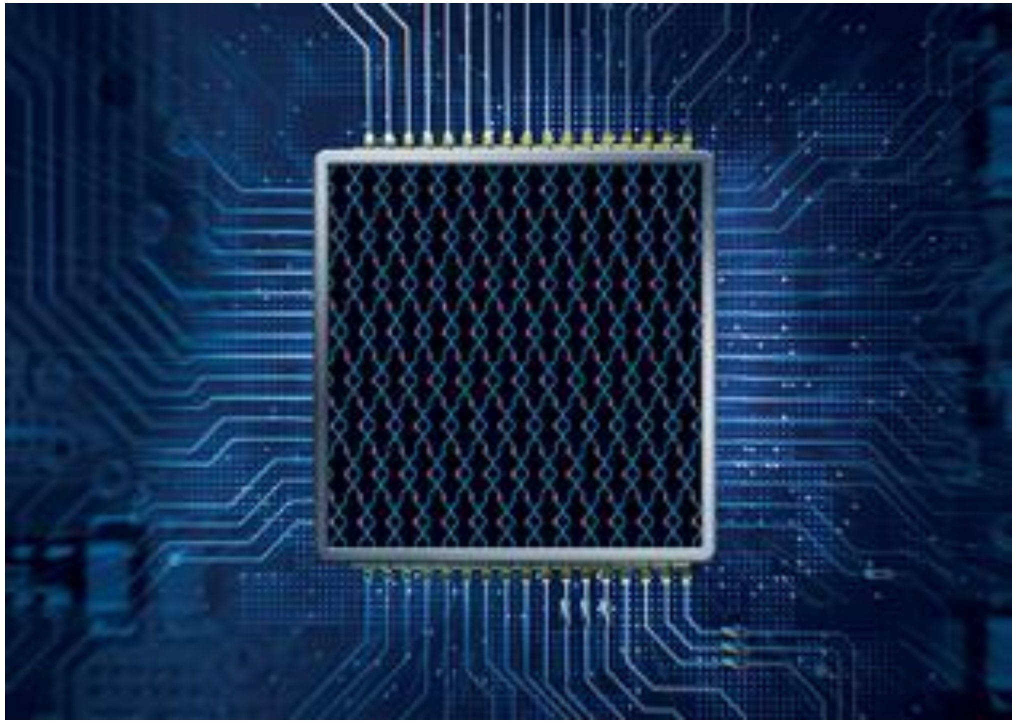
Future Technical Area – Foundry Users

Anticipated Future Solicitation

This information is provided for reference only. DO NOT propose to this section.

Foundry Users

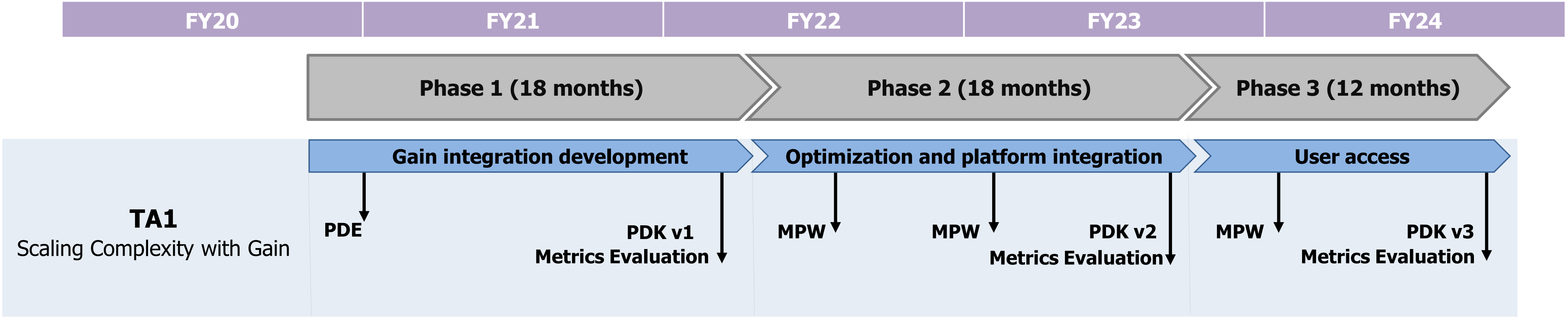
- Contribute innovative component designs
- Contribute innovative large-scale PIC system designs
- Exercise the foundry process
- Provide feedback to TA1 performers through ACAs
- Utilize PDKs and MPWs as part of their effort



Miller, Nature Photonics **11**, 403 (2017)

Foundry Users will demonstrate TA1 technology capabilities

Program Structure TA1



- **Anticipated Funding**
  - 6.2 funding
  - $40M / 48 months
  - Multiple awards
  - Cost-share anticipated

- **Major Deliverables**
  - Phase 1 – Process development evaluation (PDE), Process Development Kit (PDK) v1 release
  - Phase 2 – Chips from two multiple project wafer (MPW) runs, PDK v2 release
  - Phase 3 – Chips from one MPW run, PDK v3 release

TA1 Metrics

TA1 metric	Description	Phase 1	Phase 2	Phase 3
Active platform [(1)]	Active MPWs	-	2	1
	Active PDK release	1	1	1
	Gain block density (per reticle)	100	1,000	1,000
	Passive component density (per reticle)	1,000	10,000	10,000
Amplifier [(2)]	Saturation power	10 dBm	16 dBm	-
	Gain	20 dB	30 dB	-
	Wallplug efficiency	5%	10%	-
	Noise figure	10 dB	6 dB	-
Laser [(3)]	Optical power	0 dBm	13 dBm	16 dBm
	Wallplug efficiency	10%	25%	40%
	Maximum operating temperature, T_{max}	> 60°C	> 90°C	> 120°C
	Lifetime (hours at T_{max})	> 1,000	> 1,000	> 100,000
Passive waveguide	SiN waveguide loss	0.2 dB/cm	0.05 dB/cm	-
	Resonator quality factor, Q	1 M	10 M	-

[1)] Foundry capability shall be accessible to designers through a complete PDK, with MPW offerings fabricated on ≥ 8” wafers.

Active PDK release shall include amplifier and laser components and shall permit tailoring of integrated gain block characteristics to enable additional, customized active components. Passive components shall be included in the PDK. Passive elements include all non-gain components, including waveguides, splitters, chip couplers, phase and amplitude modulators, and integrated detectors, all demonstrating performance consistent with SoA.

Gain blocks are defined as individually-addressable, electrically-driven light emitters that demonstrate optical amplification into a passive waveguide mode. Optical gain spectrum shall operate across a 30 nm span, defined by full-width half-maximum of photoluminescence spectrum or similar metrology, within the range of 1250 nm to 1600 nm as specified by proposers. Operation of gain blocks may be demonstrated through a combination of on-chip testing and characterization with external components.

The gain block density metric may be met by demonstrating a proportional number of gain blocks on at least one quarter of the reticle (e.g. 250 gain blocks in Phase 2), with the remainder of the reticle devoted to test structures and/or MPW designs as identified by the proposer. The government considers an approximately 2.5 cm x 2.5 cm repeated wafer area to represent a reticle. Significant departures from this concept should be noted in proposals.

[(2)] Amplifier power levels are measured on-chip in passive waveguide. Small-signal gain assumes -30 dBm input power.

[(3)] Laser shall operate with a single mode and >30 dB side-mode suppression ratio. Optical power is specified on chip. Accelerated lifetime testing is permissible provided sufficient evidence is provided to support reliability assertions. Wallplug efficiency should include all critical power-consuming elements required for laser operation, including I-V drive power, control power (if needed), cooling power (if needed), coupling loss into waveguide, and other optical loss elements.

TA2: High Power Gain

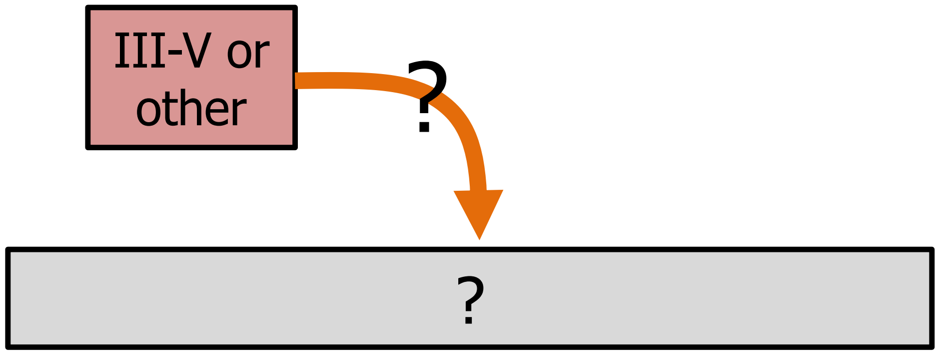
Objectives

- Establish **specialty high-power and high-speed photonics platforms** through heterogeneous integration
- Demonstrate **single-chip optical microsystems** achieving a DoD-relevant high-power function

Key Metrics and Deliverables

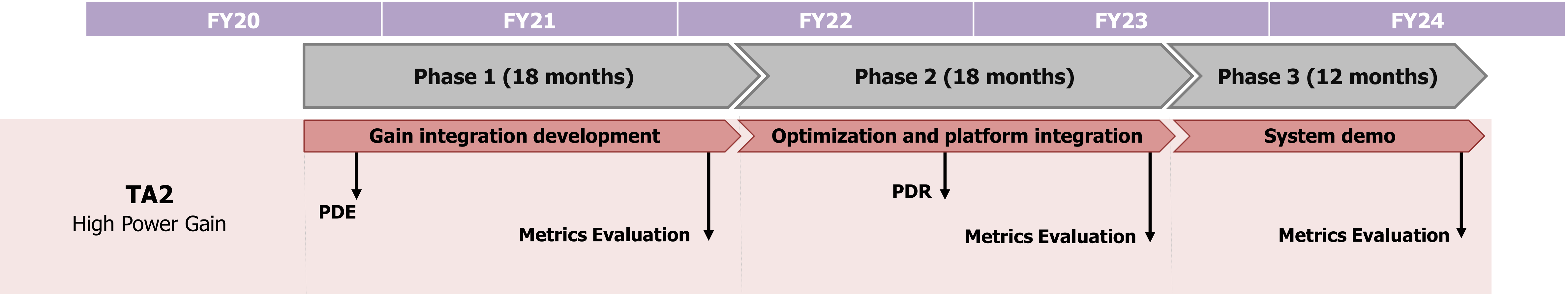
- Demonstrate **high-power integrated lasers & amplifiers**
  - output power 30 dBm (beyond SOTA)
  - low intensity & phase noise (-175 dBc/Hz, 1 kHz)
- Integrate **fast analog modulators and photodetectors**
  - f_{3dB} > 110 GHz
- Demonstrate **DoD-relevant application** on complete platform
  - Including 100 integrated components
  - Utilizing > 1 W of on-chip optical power

Specialty High-Power / Low-Loss Capability



TA2 will enable DoD-relevant applications by scaling optical power and modulation bandwidth

Program Structure TA2



- **Anticipated Funding**
  - 6.2 funding
  - $15M / 48 months
  - Multiple awards

- **Major Deliverables**
  - Phase 1 – Process development evaluation (PDE); integrated laser included in test structure chips
  - Phase 2 – Integrated laser, amplifier and active platform components in test structure chips; preliminary design review (PDR) of system demo
  - Phase 3 – Integrated laser, amplifier and active platform components in system demo chips; detailed plan for technology transition

TA2 Metrics

TA2 metric	Description	Phase 1	Phase 2	Phase 3
Laser (1)	Output power	20 dBm	27 dBm	30 dBm
	Linewidth	1 MHz	10 kHz	1 kHz
	Wallplug efficiency	10%	20%	40%
	Relative intensity noise	-145 dBc/Hz	-160 dBc/Hz	-175 dBc/Hz
Amplifier (2)	Saturation power	20 dBm	33 dBm	-
	Gain	20 dB	20 dB	-
	Wallplug efficiency	5%	10%	-
	Noise figure	10 dB	6 dB	-
Active platform (3)	RF bandwidth	50 GHz	80 GHz	110 GHz
	Waveguide loss	1 dB/cm	0.5 dB/cm	0.2 dB/cm
System demo (4)	Total component count	-	-	> 100
	Total optical power	-	-	> 1 W

(1) Laser shall be electrically-driven and operate in a single mode with >30 dB side-mode suppression ratio. Optical power is specified on chip. Wallplug efficiency should include all critical power-consuming elements required for laser operation, including I-V drive power, control power (if needed), cooling power (if needed), coupling loss into waveguide, and other optical loss elements.

(2) Amplifier power levels are measured on-chip in passive waveguide. Small-signal gain assumes -30 dBm input power.

(3) Active platform shall include a full complement of passive waveguides, splitters, chip couplers, phase and amplitude modulators, and integrated detectors, all demonstrating performance consistent with state-of-the-art. 3-dB RF bandwidth applies to both phase modulators and integrated detectors, which shall be compatible with operation at the laser output power level specified for each phase. Waveguide loss is measured at laser output power level.

(4) System demo shall be a compelling user-defined application that leverages the unique platform capabilities of on-chip, high-power gain, and a high-bandwidth integrated platform, consistent with domains of interest defined in the BAA.

Component count includes all integrated active and passive elements. Total optical power includes the contribution from all on-chip lasers and amplifiers.

TA3: Broad Spectrum Gain

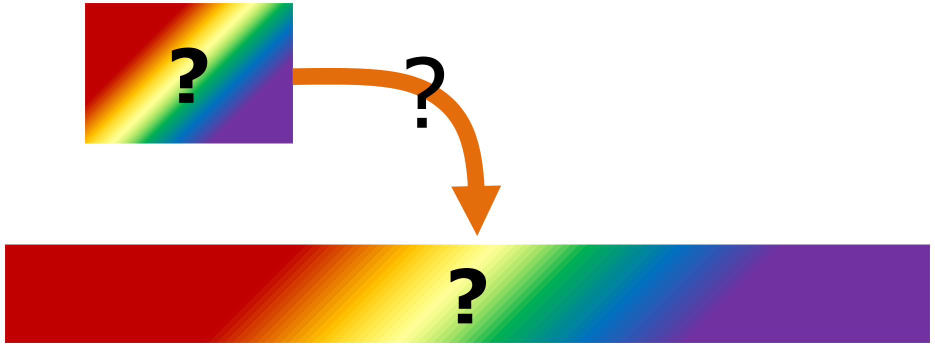
Objectives

- Establish **specialty visible to near-IR photonics platforms** through heterogeneous integration
- Demonstrate **single-chip optical microsystems** achieving a DoD-relevant function

Key Metrics and Deliverables

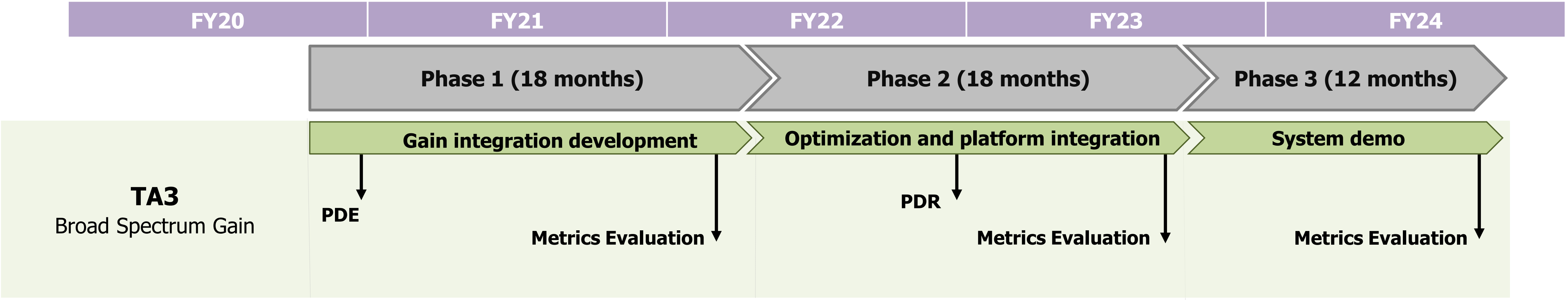
- Demonstrate **broad spectral access** from single platform
  - 8 sources per chip at different wavelengths
  - wavelength ***by design*** across visible to near-IR (400-900 nm)
- Demonstrate **high performance laser sources**
  - power 16 dBm at >1% efficiency
  - linewidth <100 Hz (beyond SOTA)
- Demonstrate **DoD-relevant application** on complete platform
  - Including 100 integrated components
  - Utilizing > ½ octave of TA3 spectrum

Specialty Broad-Spectrum / Low-Noise Capability



TA3 will enable breakthrough applications with integrated visible photonics

Program Structure TA3



- **Anticipated Funding**
  - 6.2 funding
  - $15M / 48 months
  - Multiple awards

- **Major Deliverables**
  - Phase 1 – Process development evaluation (PDE); integrated laser included in test structure chips
  - Phase 2 – Integrated laser, amplifier and active platform components in test structure chips; preliminary design review (PDR) of system demo
  - Phase 3 – Integrated laser, amplifier and active platform components in system demo chips; detailed plan for technology transition

TA3 Metrics

TA3 metric	Description	Phase 1	Phase 2	Phase 3
Laser [(1)]	Number of Wavelengths	4	6	8
	Linewidth	1 MHz	1 kHz	100 Hz
	Output power	0 dBm	10 dBm	16 dBm
	Wallplug efficiency	-	0.1%	1%
	Laser tuning range	-	1%	1%
Active platform [(2)]	Component functionality	passive across spectrum	active across spectrum	-
	Waveguide loss	6 dB/cm	1 dB/cm	-
System demo [(3)]	Total component count	-	-	> 100
	System spectral bandwidth	-	-	> half octave

[(1)] Performers shall enable laser operation at wavelengths by design at any point in the spectral window from 400 nm to 900 nm without recurring customization of the photonics platform. Target wavelengths will be provided by DARPA at the beginning each phase. Laser shall be electrically-driven and operate in a single mode with a side-mode suppression ratio > 30 dB. Optical power is measured on-chip. Wallplug efficiency should include all critical power-consuming elements required for laser operation, including I-V drive power, control power (if needed), cooling power (if needed), coupling loss into waveguide, and other optical loss elements.

[(2)] Platform shall include a full complement of passive waveguides, splitters, and chip couplers in Phase 1. Active components, including phase modulators, amplitude modulators, and integrated detectors, shall be included in Phase 2. All components shall demonstrate performance consistent with state of the art and function across the entire spectral access range. Waveguide loss applies to the entire spectral access range.

[(3)] System demo shall be a compelling user-defined application that leverages the unique platform capabilities of broad spectrum access on a complete integrated platform, consistent with domains of interest defined in the BAA.

Component count includes all integrated active and passive elements. System spectral bandwidth defined by the use of multiple optical sources spanning at least one half-octave range.

Important Proposal Elements

- **Gain concept (all TAs)**
- **Heterogeneous integration plan (all TAs)**
- **Optical isolation strategy (all TAs)**
- **Gain component performance analysis (all TAs)**
  - laser and amplifier WPE
- **Thermal analysis (TA2)**

- **Platform performance capabilities (all TAs)**
  - other active and passive components
- **Risks & mitigation (all TAs)**
- **Manufacturing (TA1)**
  - yield, lifetime, and process control

- **Plans to enable designers (TA1)**
  - PDK contents & EDA tools
- **Plans to provide access (TA1)**
  - MPW schedule and approach
- **System demonstration (TA2 & TA3)**
  - quantitative comparison to state-of-the-art

Include everything in wall-plug efficiency estimates

- I-V drive power
- Control power (if needed)
- Cooling power (if needed)
- Coupling loss into waveguide
- All other power-consuming elements
- All other optical loss elements

Include all components required for general PICs

- Modulators
- Detectors
- Waveguides
- Splitters
- Etc.

Important Dates

- BAA Posting Date: November 18, 2019
- Proposers Day: November 20, 2018
- Abstract Due Date: **December 11, 2019 at 1:00 PM**
- FAQ Submission Deadline: January 24, 2020 at 1:00 PM
  - DARPA will post a consolidated Question and Answer (FAQ) document on a regular basis. To access the posting go to: http://www.darpa.mil/work-with-us/opportunities.
- Proposal Due Date: **February 7, 2020 at 1:00 PM**
- Estimated period of performance start: July 1, 2020

Questions: HR001120S0008@darpa.mil

Evaluation Criteria, in Order of Importance

1. Overall Scientific and Technical Merit
   - Demonstrate that the proposed technical approach is innovative, feasible, achievable, and complete.
   - Describe how the proposed approach will achieve each program metric with sufficient detail and supporting experimental measurements, modeling, calculations, and/or simulations.
2. Potential Contribution and Relevance to the DARPA Mission
   - Note the updated wording, with an emphasis on contribution to U.S. national security and U.S. technological capabilities.
3. Cost Realism
   - Ensure proposed costs are realistic for the technical and management approach and accurately reflect the goals and objectives of the solicitation.
   - Verify that proposed costs are sufficiently detailed, complete, and consistent with the Statement of Work.
   - For efforts with a likelihood of commercial application, the level of performer cost share will be considered as a significant element of the Cost Realism evaluation.

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